

Rev. V4

Features

- High Gain: 21 dBOutput P1dB: 20 dBm
- · Variable Gain with Adjustable Bias
- Lead-Free 3 mm QFN Package
- Halogen-Free "Green" Mold Compound
- RoHS* Compliant

Description

The MAAM-010651 is a 3-stage, buffer amplifier with a 20 dBm output P1dB. The surface mount 3 mm QFN package allows easy assembly. This amplifier is fully matched to 50 ohms on both the input and output. It is designed for use as an LO buffer amplifier stage or as a driver amplifier in transmit chains and is ideally suited for 38 GHz band point-to-point radios.

Each device is 100% RF tested to ensure performance compliance. The part is fabricated using an efficient PHEMT process.

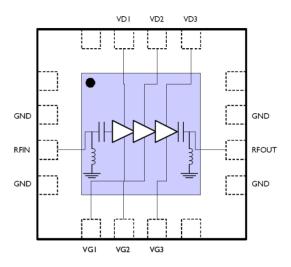
The MTTF is >1,000,000 hours at a 150°C junction temperature.

Ordering Information¹

Part Number	Package	
MAAM-010651-000000	Bulk Packaging	
MAAM-010651-TR0500	500 Piece Reel	
MAAM-010651-TR1000	1000 Piece Reel	
MAAM-010651-000SMB	Sample Evaluation Board	

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration^{2,3}

Pin No.	Function	Pin No.	Function	
1	No Connection	9 Ground		
2	Ground	10	RF _{OUT}	
3	RF _{IN}	11	11 Ground	
4	Ground	12	No Connection	
5	V _G 1	13	V _D 3	
6	V _G 2	14 V _D 2		
7	V _G 3	15 V _D 1		
8	No Connection	16 No Connection		
		Paddle ³	Ground	

- MACOM recommends connecting unused package pins to ground.
- 3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

^{*} Restrictions on Hazardous Substances, European Union Directive 2011/65/EU

MAAM-010651



Amplifier, Buffer 37 - 40 GHz

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Electrical Specifications:

Freq. 37 - 40 GHz, $T_B = 30^{\circ}C^4$, $V_{DD} = 4$ V, $I_{DQ} = 250$ mA⁵, $P_{in} = -14$ dBm, $Z_0 = 50$ Ω

Parameter	Units	Min.	Тур.	Max.
Input Return Loss	dB	_	7	_
Output Return Loss	dB	_	10	_
Small Signal Gain	dB	17	21	24.5
Reverse Isolation (S12)	dB	_	40	_
Output P1dB	dBm	_	20	_
Output IP3 (@ +4 dBm SCL)	dBm	27	30.5	_
P _{SAT}	dBm	19.5	22	_

^{4.} T_B = MMIC Base Temperature

Maximum Operating Ratings^{6,7}

Parameter	Absolute Maximum		
Input Power	+20 dBm		
Drain Supply Voltage	+4.3 V		
Gate Supply Voltage	-1.5 to 0 V		
Operating Temperature	-40°C to +85°C		
Junction Temperature	+150 °C		
Storage Temperature	-55°C to +150°C		
ESD Machine Model	Class A		
ESD Human Body Model	Class 1A		
MSL	MSL3		

Exceeding any one or combination of these limits may cause permanent damage to this device.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

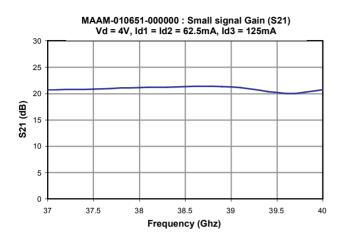
^{5.} Adjust V_{GG} between -1.0 and -0.1 V to achieve specified I_{DO}.

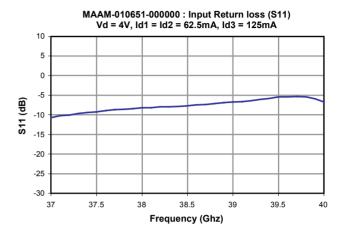
MACOM does not recommend sustained operation near these survivability limits.

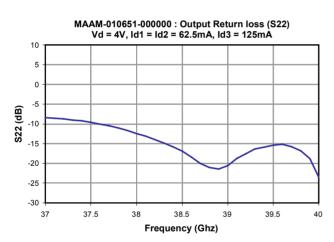


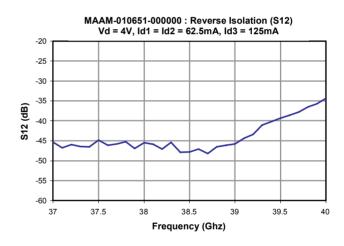
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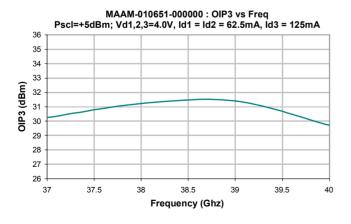
Typical Performance Curves

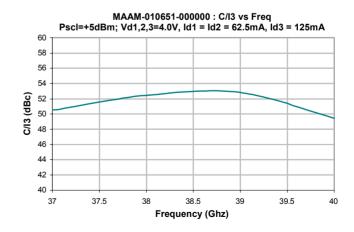








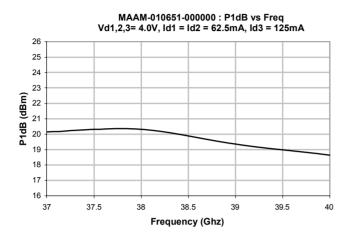


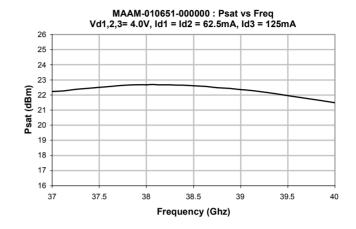




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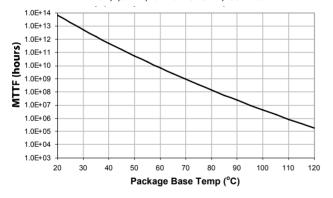
Typical Performance Curves (cont.)

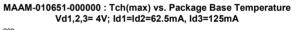


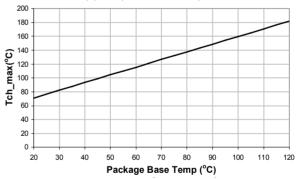


MTTF

MAAM-010651-000000 : MTTF hours vs. Package Base Temperature Vd1,2,3= 4V; ld1=ld2=62.5mA, ld3=125mA







MAAM-010651-000000 : Operating Power De-rating Curve (continuous) 2.0 1.8 1.6 **N** 1.2 1.0 0.8 0.6 0.4 0.2 0.0 90 100 110 120 130 140 150 20 30 40 50 60 80 Package Base Temp (°C)

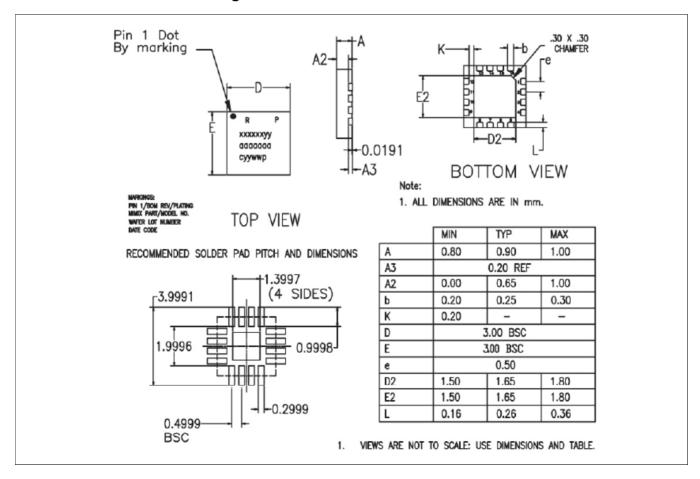


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App Note [1] Biasing - It is recommended to bias the amplifier with V_D = 4 V and I_{D_TOTAL} = 250 mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.3 V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement - Each DC pin $(V_D \text{ and } V_G)$ needs to have DC bypass capacitance (100 pF/10 nF/1 μ F) as close to the package as possible.

Lead-Free 3 mm QFN Package



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